



Hdl Chip Design: A Practical Guide for Designing, Synthesizing & Simulating Asics & Fpgas Using Vhdl or Verilog

By Douglas J. Smith

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- Sales Rank: #330448 in Books
- Published on: 1998-03
- Ingredients: Example Ingredients
- Original language: English
- Number of items: 1
- Dimensions: 11.42" h x 28.70" w x 21.85" l,
- Binding: Hardcover
- 448 pages

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Editorial Review

Review

Arthur C. Clarke once wrote that any sufficiently advanced civilization would possess seemingly magical powers to a lesser-advanced one. Technology, and in particular computer technology, has and always will present a Janus head to the world. While delivering enormous capability and freedom, the instrumentality by which that freedom is delivered becomes even more arcane and obscurantist to the users of that technology. The backyard auto mechanic is an artifact. We are all, including most mechanics, relegated to simply filling the gas tank, changing the oil or replacing the occasional black box. And what of those practitioners of these arcane arts, who in designing and building the devices which channel electrons to the exacting demands of industry and consumers seem to take on almost a mantle of priesthood? Any priesthood needs a catechism, and Douglas J. Smith's HDL Chip Design might well fit that role. This publication is designed as an introduction to and reference on using the two industry standard hardware description languages (HDL's) VHDL and Verilog to design, simulate and synthesize Applications-Specific Integrated Circuits (ASIC) and Field Programmable Gate-Arrays (FPGA). Emphasis for modeling is at the RT (register transfer) level, using a top-down design method. This reviewer approached this text as a student with a physics background and an interest in glimpsing the inner sanctum of chip design and came away impressed with its clarity, depth, and no-nonsense approach. This is not a book for the fainthearted neophyte, but a challenging and rewarding introduction to HDL chip design, and a treasury as a reference book to the practicing professional. -- *From Independent Publisher*

Users Review

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Claire Underwood:

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Effie Phillips:

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